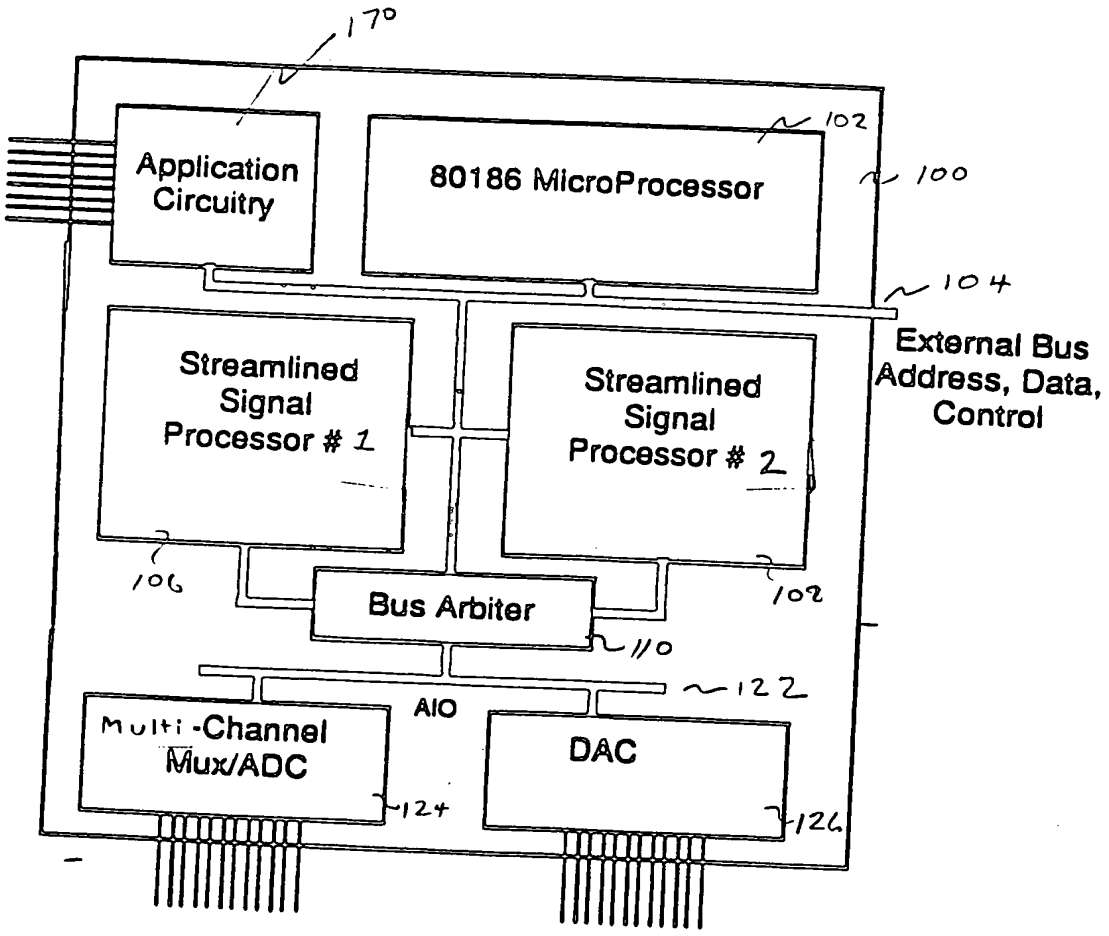
170
Application Circuitry
80186 MicroProcessor
102
100
104
External Bus Address, Data, Control
Streamlined Signal Processor # 1
Streamlined Signal Processor # 2
106
108
Bus Arbiter
110
122
AIO
Multi-Channel Mux/ADC
124
DAC
126

FIGURE 1a

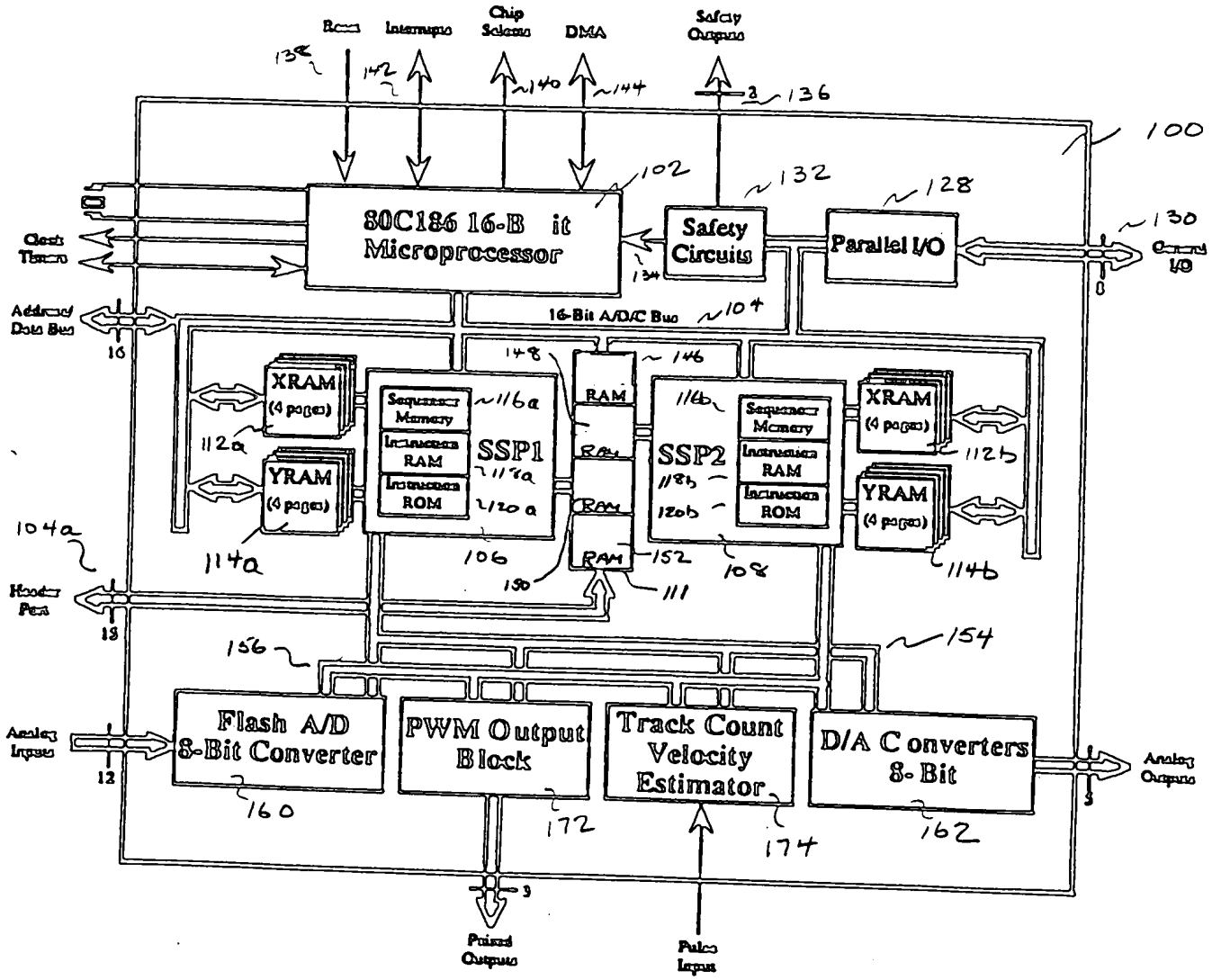
Resets
Interrupts
Chip Selects
DMA
Safety Outputs
138
142
140
144
136
100
102
132
128
130
80C186 16-Bit Microprocessor
Safety Circuits
Parallel I/O
Clock Timers
134
Address Data Bus
16
16-Bit A/D/C Bus
104
148
146
XRAM (4 pages)
112a
YRAM (4 pages)
114a
Sequencer Memory
Instruction RAM
Instruction ROM
SSP1
116a
118a
120a
RAM
SSP2
116b
118b
120b
XRAM (4 pages)
112b
YRAM (4 pages)
114b
104a
Header Pins
18
106
150
152
111
108
156
154
Analog Inputs
12
Flash A/D 8-Bit Converter
160
PWM Output Block
172
Track Count Velocity Estimator
174
D/A Converters 8-Bit
162
Analog Outputs
3
Paired Outputs
Pulse Inputs

FIGURE 1b

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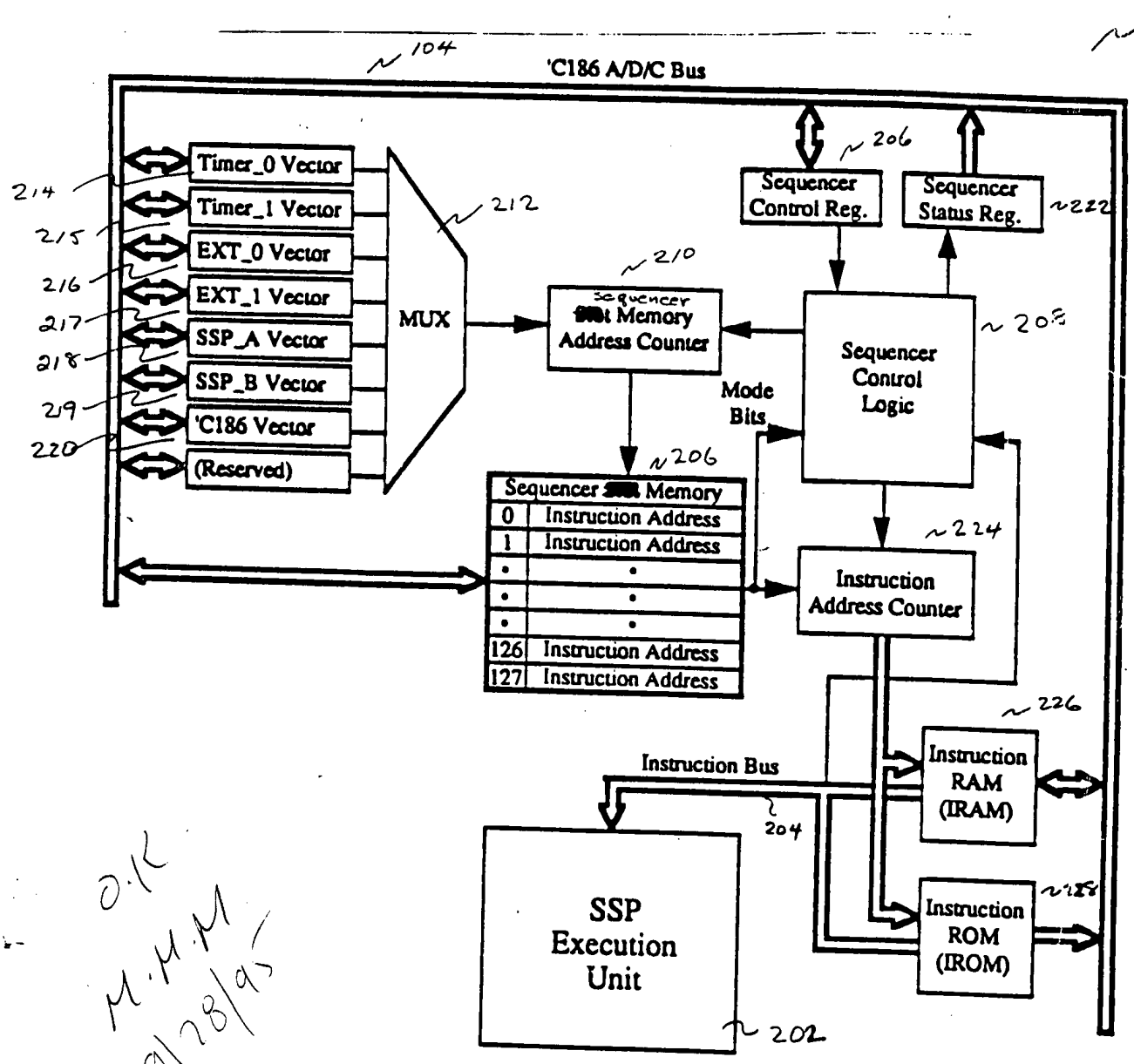

O.K
M.M.M
9/28/95

FIGURE 2

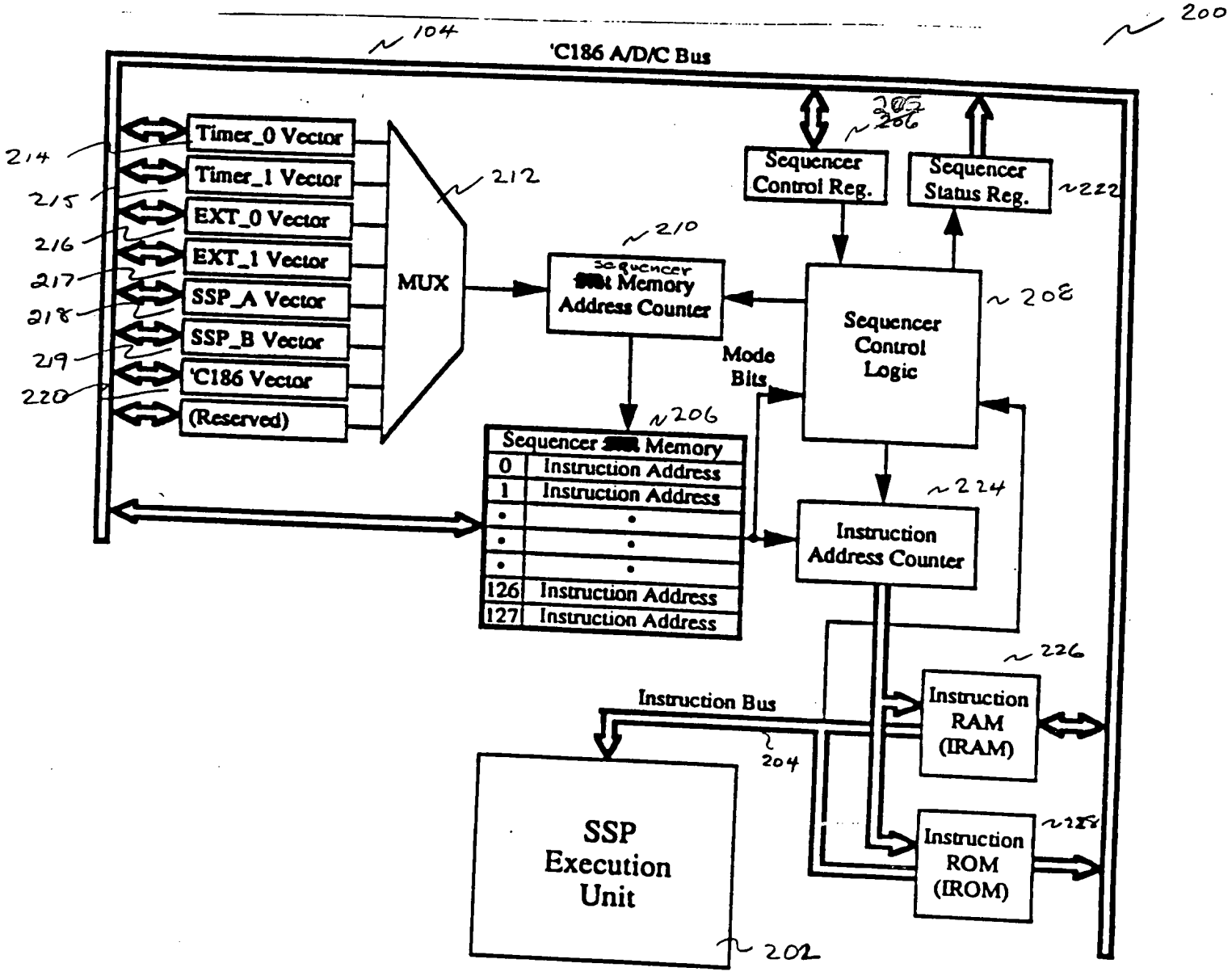
200
104
'C186 A/D/C Bus
Timer_0 Vector
Timer_1 Vector
EXT_0 Vector
EXT_1 Vector
SSP_A Vector
SSP_B Vector
'C186 Vector
(Reserved)
214
215
216
217
218
219
220
MUX
212
Sequencer Control Reg.
Sequencer Status Reg.
222
Sequencer Memory Address Counter
210
Sequencer Control Logic
208
Mode Bits
Sequencer Memory
206
0 Instruction Address
1 Instruction Address
126 Instruction Address
127 Instruction Address
224
Instruction Address Counter
226
Instruction Bus
204
Instruction RAM (IRAM)
Instruction ROM (IROM)
SSP Execution Unit
202

FIGURE 2

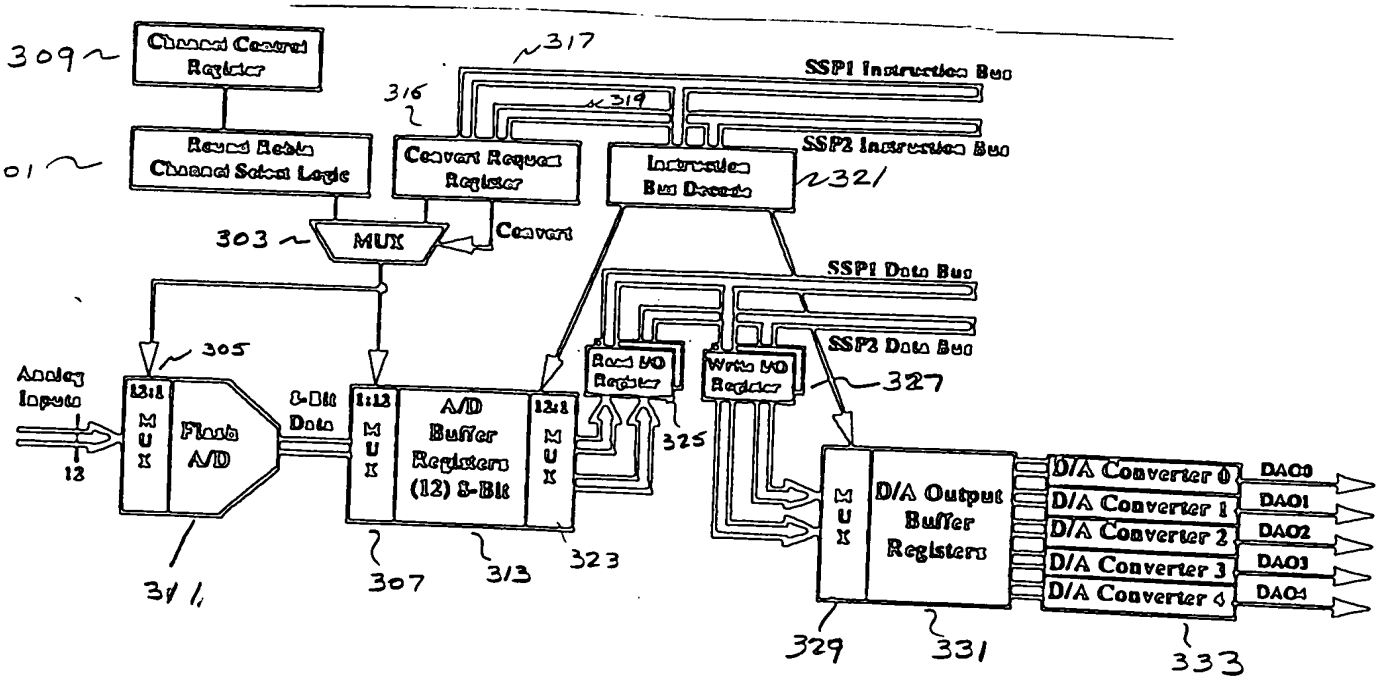
309
Channel Control Register
317
SSP1 Instruction Bus
316
319
301
Round Robin Channel Select Logic
Convert Request Register
SSP2 Instruction Bus
Instruction Bus Decode
321
303
MUX
Convert
SSP1 Data Bus
SSP2 Data Bus
305
Analog Inputs
12
12:1 MUX
Flash A/D
8-Bit Data
1:12 MUX
A/D Buffer Registers (12) 8-Bit
12:1 MUX
Read I/O Register
Write I/O Register
325
327
MUX
D/A Output Buffer Registers
D/A Converter 0
D/A Converter 1
D/A Converter 2
D/A Converter 3
D/A Converter 4
DAC0
DAC1
DAC2
DAC3
DAC4
311
307
313
323
329
331
333

FIGURE 3

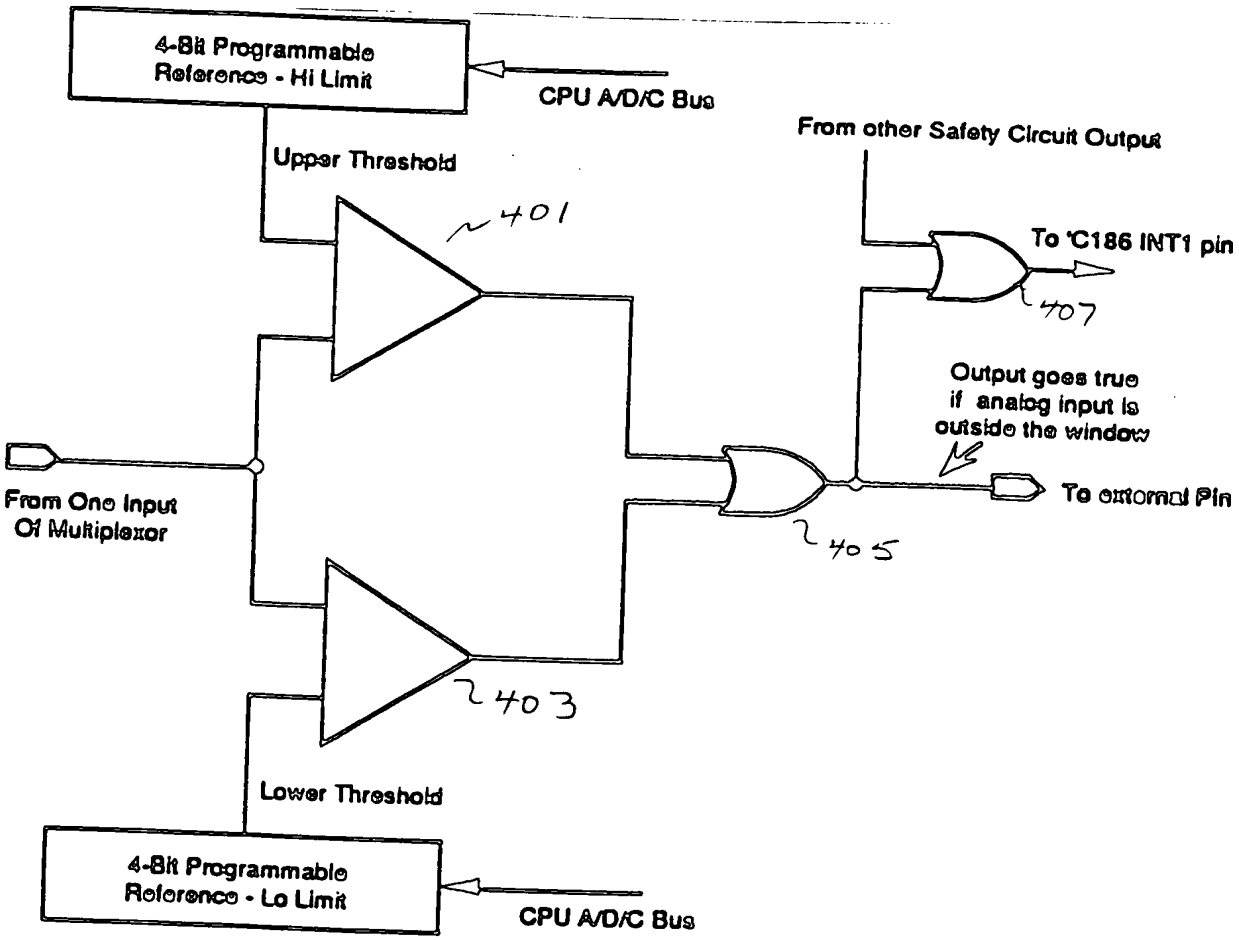
4-Bit Programmable Reference - Hi Limit
CPU A/D/C Bus
Upper Threshold
401
From other Safety Circuit Output
To 'C186 INT1 pin
407
Output goes true if analog input is outside the window
To external Pin
From One Input Of Multiplexor
405
403
Lower Threshold
4-Bit Programmable Reference - Lo Limit
CPU A/D/C Bus

FIGURE 4

Resolution Digital Code	8 bits Unipolar, magnitude only

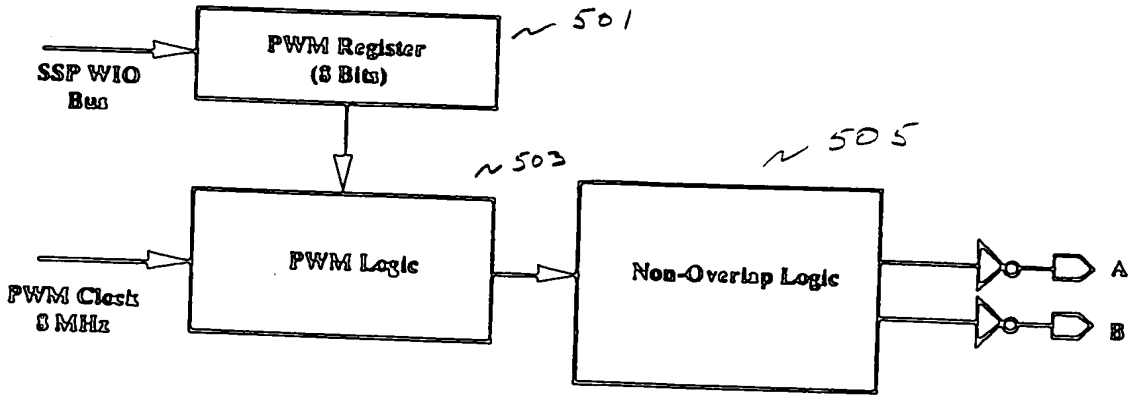

FIGURE 5a

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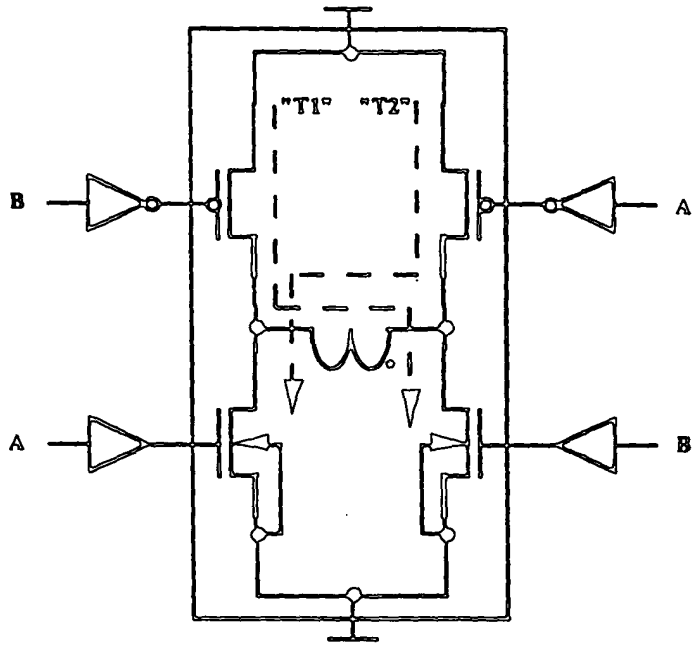

Figure 5b Typical Driver Connected to PWM Output

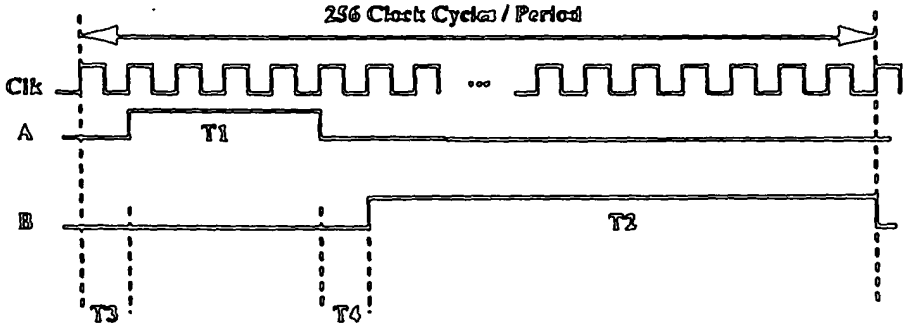

Figure 5c Pulse-Width Modulation Timing

Notes:
1 cycle = 125ns
1 cycle ≤ T1 ≤ 253 cycles
T3 = T4 = 1 cycle (Non-Overlap Delay Time)
T2 = (256 - 2 - T1) cycles

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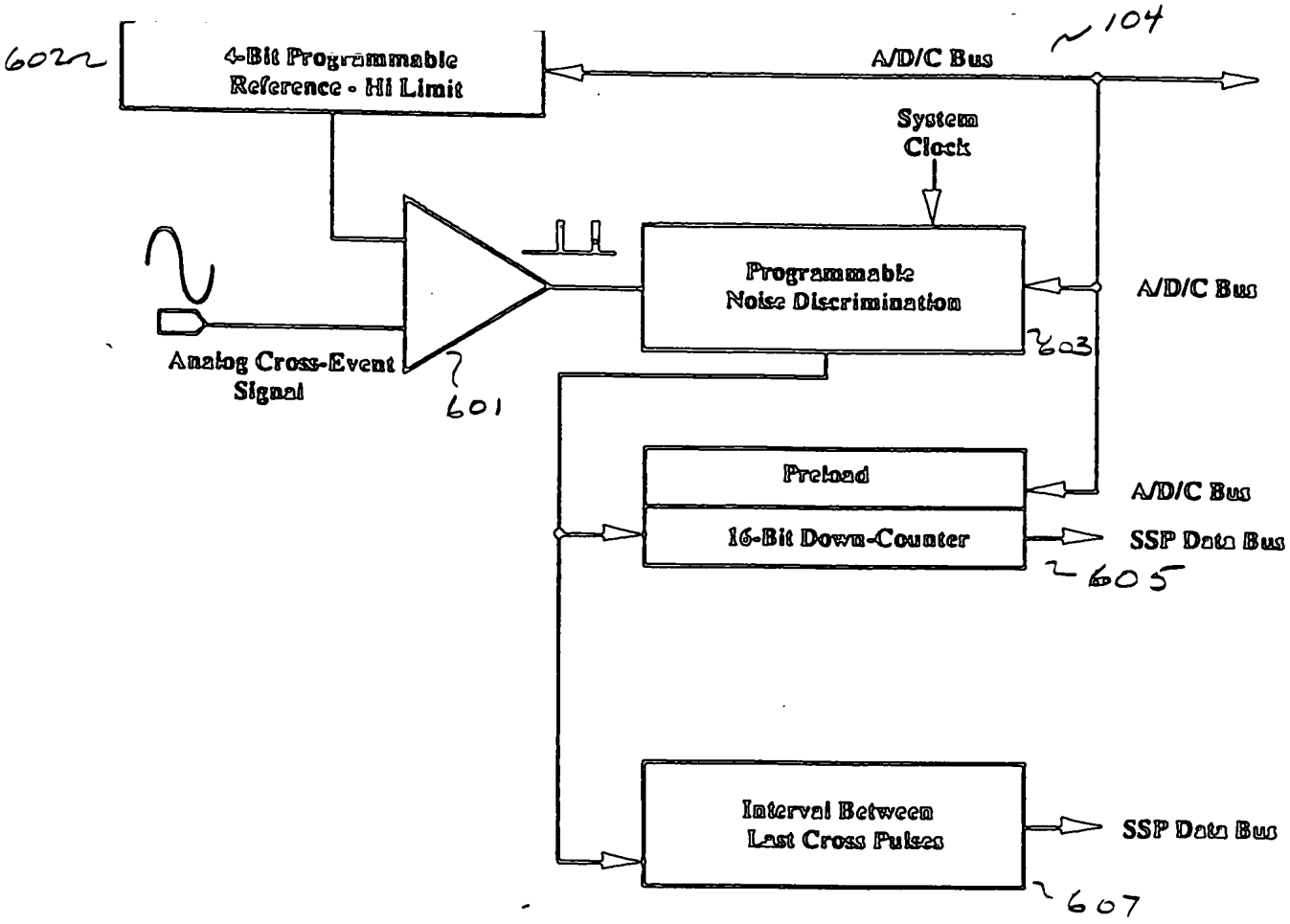

FIGURE 6